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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,444	12/31/2003	Jeung-Hie Choi	51876P555	1775

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EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,444	CHOI, JEUNG-HIE	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toba (US 2002/0137551) in view of Kurashima (US 2003/0063041).

Regarding **Claim 1**, Toba teaches a display apparatus, comprising:

a plurality of display panels, each showing different display (Toba, Fig. 7 elements 5 and 11);

a single display panel driving unit for commonly operating the plurality of display panels (Toba, Fig. 7 elements 6, 21-25, 27 and 28);

a connection switch for physically and electrically inter-connecting the single display panel driving unit with the display panels (Toba, Fig. 7 elements 27 and 28),

wherein the display panel driving unit includes:

a display panel driver shared by the display panels (Toba, Fig. 7 element 25, 5 and 11); and

a display path control unit for controlling the display panel driver (Toba, Fig. 7 elements 6, 21-23),

wherein the display panel driver is enabled by the display path control unit according to which one of the plurality of display panels are activated (Toba, Fig. 7 elements 6, 21 and 25 the control circuit tells the driver which display is being driving and what signals to provide to the display).

Toba fails to teach wherein a different portion of the display panel driver is enabled by the display path control unit according to which one of the plurality of display panels are activated. Kurashima teaches wherein a different portion of a display panel driver is enable according to which one of the plurality of display panels are activated (Kurashima, Fig. 5 element 7, Pg. 2 paragraph [0025]). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the display path control unit of Toba to control the display panel driver to enable a different portion depending on which one of the plurality of display panels are activated as taught by Kurashima in order to allow for different resolution displays for the plurality of panels as well as to save power.

Regarding **Claim 2**, Toba further teaches that the display panels includes a first display panel and a second display panel, and rear sides of the first and second display panels face each other (Toba, Figs. 1, 2 and 7 elements 5 and 11). Toba as modified above fails to teach that the display panel driving unit is disposed between the first and second display elements as claimed. Kurashima further teaches a display panel driving unit disposed between the first and second display elements (Kurashima, Fig. 10 elements 67a, 67b, 1D and 2D). It would have been obvious to one of ordinary skill in the art at the time of the invention to place the display panel driving unit of Toba

between the first and second display elements as taught by Kurashima in order to reduce the wire connections because the driving unit would be closer to two displays.

Regarding **Claim 3**, Toba fails to teach that the connection is formed by using chip on glass method. Kurashima teaches that the chip on glass process is well known in the art (Kurashima, Pg. 5 paragraph [0075]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use chip on glass method as taught by Kurashima to form the connection switch of Toba in order to more easily integrate the switch system into the driving IC.

Regarding **Claim 10**, Toba in view of Kurashima further teaches that the display panel driving unit is packages in a flexible U or S shape (Kurashima, Fig. 10 elements 67a, 67b, 109a and 109b).

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toba (US 2002/0137551) in view of Kurashima (US 2003/0063041) as applied to Claims 1-3, 10 and 11 above, and further in view of Kou (US 5,874,928).

Regarding **Claim 6**, Toba in view of Kurashima fails to teach that the display panel driving unit includes all the additional features as claimed. Kou teaches a display panel driving unit comprising:

a CPU interface control unit for controlling constitutional elements includes the display panel driving unit by receiving a command from an external host or a CPU (Kou, Fig. 1 element 12);

a display panel control unit for controlling the display panel with an external control signal transmitted through the CPU interface control unit or an independent port (Kou, Fig. 2 element 32);

a memory unit for storing data displayed on the display panels (Kou, Fig. 2 element 36);

X and Y address decoders for selecting a corresponding address of the memory unit by decoding an encoding signal outputted from the display panel control unit (Kou, Col. 5 lines 43-49);

a register unit for informing each independent operation condition of the display panels (Kou, Fig. 2 element 40 data serializer is equivalent to a register unit);

a timing control unit for controlling a point of time for decoding, latching an displaying a data for the corresponding display panel by the information obtained from the register unit (Kou, Fig. 2 element 52);

a line address decoder for decoding an address for the data of the corresponding display panel at a line unit by responding to an output of the timing control unit (Kou, Col. 5 lines 43-49 in order to provide data to the display panel where each row is scanned it is necessary to have a line address decoder for decoding an address for a particular row);

a latch unit for latching the data corresponding to the address decoded at the line unit wherein the data is transferred from the memory unit (Kou, Fig. 2 element 45); and

a voltage generation unit for supplying a power voltage for operating each display panel (Kou, Fig. 2 element 60).

It would have been obvious to one of ordinary skill in the art to use the display control unit as taught by Kou in place of the generic display controller of Toba in view of Kurashima in order to provide a mechanism for simultaneously driving a plurality of displays which refreshes each of the displays at an optimal refresh rate for that display and to improve performance of both displays (Kou, Col. 4 lines 41-46).

Regarding **Claim 7**, Toba as modified by Kurashima and Kou further teaches that the display panels share the X and Y address decoders, the line address decoder, the voltage generation unit, the memory unit and the register unit during a concurrent and cooperative operation (Kou, Figs. 1 and 2, Col. 4 line 45 to Col. 5 line 11).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toba (US 2002/0137551) in view of Kurashima (US 2003/0063041) and Kou (US 5,874,928) as applied to Claims 6 and 7 above, and further in view of Nikawa (US 2002/0111200).

Regarding **Claim 8**, Toba in view of Kurashima and Kou fail to teach that the voltage generation unit comprises a voltage converter and a DC/DC booster controlled by on-off states of the first and second display panels.

Nikawa teaches a voltage generation unit comprising a voltage converter and a DC/DC booster controlled by the on off state of a single display panel (Nikawa Figs. 4 and 10 element 27). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the voltage generation unit as taught by Nikawa in place of the voltage generation unit of Toba in view of Kurashima and Kou in order to be able to

monitor the activity of each display panel and decide the appropriate power output thereby saving power (Nikawa, Pg. 1 paragraphs [0015-0016]).

Response to Arguments

Applicant's arguments filed October 17th, 2007 have been fully considered but they are not persuasive.

Regarding independent Claim 1, the applicant argues that Toba in view of Kurashima fails to teach "a different portion of the display panel driver is enabled for disabled". The examiner respectfully disagrees. Kurashima clearly teaches enabling and disabling different portions of the display panel driver according to which display is being driven. Kurashima paragraph [0025] states "the drive circuit may include the functions of stopping a signal supply to the fourth electrode when the first panel is displaying; and stopping a signal supply to the second electrode when the second panel is displaying", which clearly meets the limitations as set forth in the claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 28, 2007 - kx -

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER